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Computer Circuit Operations LLC

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

COMPUTER CIRCUIT OPERATIONS LLC,

Plaintiff

v.

ARASTU SYSTEMS, INC. and ARASTU SYSTEMS PVT. LTD,

Defendants

Case No.: 5:19-cv-3719

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Computer Circuit Operations LLC ("CCO"), for its Complaint against Defendants Arastu Systems, Inc. ("Arastu-America") and Arastu Systems Pvt. Ltd ("Arastu-India") (collectively, "Arastu" or "Arastu Defendants"), hereby alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. On information and belief, Defendant Arastu-India is an Indian private limited company with a principal place of business at 301 Safal Prelude, Corporate Road, Prahlad Nagar, Ahemdabad, India.

3. On information and belief, Defendant Arastu-America is a California corporation with a principal place of business at 2690 S White Rd, Ste 245, San Jose CA 95148

JURISDICTION AND VENUE

4. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Arastu of claims of U.S. Patent Nos. 6,820,234, 7,107,386, 7,278,069, and 7,426,603 ("the Patents-in-Suit").

5. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Arastu-India pursuant to Fed. R. Civ. P. 4(k)(2).

7. Venue is proper as to Arastu-India in this district under 28 U.S.C. § 1391(c) because, *inter alia*, it is a foreign corporation.

8. Arastu-America is subject to personal jurisdiction of this Court because, inter alia, on information and belief, (i) Arastu-America is headquartered in the State of California, (ii)

Arastu-America maintains office locations in the State of California; (iii) Arastu-America is registered to transact business in the State of California; and (iv) Arastu-America has committed and continues to commit acts of patent infringement in the State of California, including by making, using, offering to sell, and/or selling accused products and services in California, and/or importing the Accused Products into California.

9. Venue is proper as to Arastu-America in this district because, inter alia, on information and belief, Arastu-America is headquartered in, and maintains a regular and established place of business, in this judicial district, and Arastu-America has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district, and/or importing accused products and services into this district.

BACKGROUND

10. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 ("the '234 Patent"), entitled "Skew Calibration Means And A Method Of Skew Calibration." A copy of the '234 Patent is attached as Exhibit A hereto.

11. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the '234 Patent.

12. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 ("the '386 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness." A copy of the '386 Patent is attached as Exhibit B hereto.

13. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the '386 Patent.

14. On October 2, 2007, the United States Patent and Trademark Office duly and

lawfully issued U.S. Patent No. 7,278,069 ("the '069 Patent"), entitled "Data transmission apparatus for high-speed transmission of digital data and method for automatic skew calibration." A copy of the '069 Patent is attached as Exhibit C hereto.

15. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the '069 Patent.

16. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 ("the '603 Patent"), entitled "Memory Bus Arbitration Using Memory Bank Readiness." A copy of the '603 Patent is attached as Exhibit D hereto.

17. Stephen Clark Purcell and Scott Kimura invented the technology of the '603 Patent.

18. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

19. By letter dated April 30, 2019, CCO notified Arastu-America of the existence of the Patents-in-Suit, and of direct and induced infringement by Arastu. CCO's letter identified exemplary infringing Arastu products and an exemplary infringed claim for each of the Patents-in-Suit.

20. As of the date of this Complaint, CCO has not received any response from Arastu.

21. Accordingly, Arastu has received notice of the Patents-in-Suit and of direct and induced infringement thereof by Arastu.

COUNT I: INFRINGEMENT OF THE '234 PATENT

22. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

23. On information and belief, the Arastu Defendants have, individually, and jointly,

infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Arastu DDR3, LPDDR3, DDR4, and LPDDR4 Memory Controllers ("Accused Arastu Products").

24. For example, on information and belief, Arastu has infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Arastu Products. *See* Arastu LPDDR3/4 DRAM Memory Controller Datasheet, Ex. 1 at 1 (showing the Initialization and Training Control block connected to LPDDR PHY via the DFI Training interface; "Supports all LPDDR3/4 commands and trainings"). Accused Arastu Products initiate Write Leveling and Read Optimization. *See Id. See also* Ex. 2, LPDDR4, JESD209-4B, Feb. 2017, pp. 186, 190-194. The PHY comprises at least one driving register for latching transmitted signals, with a plurality of input and outputs. The PHY further comprises at least one receiving register for latching received signals, with a plurality of inputs and outputs. The memory controller comprises a main clock for generating a main clock signal. Ex. 2, LPDDR4, JESD209-4B, Feb. 2017, p. 17. The PHY further comprises a reference clock for generating a reference signal for calibrating the receiving register, such as during DQ Read Training. *See* Ex. 2, LPDDR4, JESD209-4B, Feb. 2017, p. 190. The reference clock is associated with the main clock. The PHY further comprises a first set of phase shift means associated with said driving register, such as phase shift circuitry, for the relative alignment of the driving signals' timing, such as the circuitry of the PHY supporting the write leveling feature. *Id.* at 186 ("4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every

DQS input signal during Write Training Mode. The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO. 5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings. 6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.").

25. On information and belief, Arastu has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, DDR3, LPDDR3, DDR4, and LPDDR4 systems that incorporate the Accused Arastu Products. Arastu had the knowledge of the '234 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Arastu Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

26. On information and belief, Arastu has committed the foregoing infringing activities without a license.

27. On information and belief, Arastu's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

28. On information and belief, Arastu knew the '234 Patent existed, knew of an exemplary infringed claim of the '234 Patent, and knew of exemplary infringing Arastu products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT II: INFRINGEMENT OF THE '386 PATENT

29. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

30. On information and belief, the Arastu Defendants have, individually, and jointly, infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Arastu Products.

31. For example, on information and belief, Arastu has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States an apparatus adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. *See, e.g.*, Arastu LPDDR3/4 DRAM Memory Controller, p. 1, Ex. 1. DDR3/4 Memory to which the Accused Arastu Products connect has multiple memory banks. The Accused Arastu Products send the requests over a memory bus. Ex. 1 at 2 ("Maximizes DAM bus utilization . . ."). The Accused Arastu Products comprise a queue comprising a plurality of request stations for storing memory transactions, such as read requests. *See* Ex. 1 at 1. Each of the memory transactions is addressed to one of the memory banks. The Accused Arastu Products include an arbiter, such as the Command Buffer, the Bank Management Unit, and/or the DFI Interface. *See* Ex. 1 at 1. Arastu's arbiter is simultaneously coupled to each of the request stations and adapted to select any of the memory transactions. *See* Ex. 1 at 2 ("Maximizes DRAM bus utilization by implementing Look-Ahead command processing and Bank Management"). The arbiter is configured to generate a plurality of bank readiness signals, such as following the submission of an activate command to the DDR4 memory. Arastu's arbiter, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. Ex. 1 at 2. ("Maximizes DRAM bus utilization by implementing Look-Ahead command processing and Bank Management").

32. On information and belief, Arastu has induced, and continues to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, DDR3, LPDDR3, DDR4, and LPDDR4 systems that incorporate the Accused Arastu Products. Arastu had the knowledge of the '386 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Arastu Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

33. On information and belief, Arastu has committed the foregoing infringing activities without a license.

34. On information and belief, Arastu's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

35. Arastu knew the '386 Patent existed, knew of its claims, and knew of Arastu infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT III: INFRINGEMENT OF THE '069 PATENT

36. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

37. On information and belief, the Arastu Defendants have, individually, and jointly, infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Arastu Products.

38. For example, on information and belief, Arastu has infringed at least claim 12 of

the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus, including during development, design, testing, and verification of the Accused Arastu Products. *See* Arastu LPDDR3/4 DRAM Memory Controller Datasheet, Ex. 1 at 1 (showing the Initialization and Training Control block connected to LPDDR PHY via the DFI Training interface; "Supports all LPDDR3/4 commands and trainings"). Accused Arastu Products initiate Write Leveling and Read Optimization. *See Id. See also* Ex. 2, Ex. 2, LPDDR4, JESD209-4B, Feb. 2017, pp. 186, 190-194. Arastu calibrates registers of the receiver, such as the receiving PHY registers in relation to a reference clock edge. Arastu calibrates propagation delays of registers of the transmitter, using the calibrated registers of the receiver with the Write Leveling feature. *Id.* at 186 ("The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller."). The calibration is performed by measuring time offsets between different signals that form a communication channel, including the DQS_t-DQS-c and CK_t-CK_c signals. The calibration is performed for a plurality of data patterns, such as DQS_t – DQS_c patterns with variable delays. *Id*. at 186 ("The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair."). Arastu applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. *See Id.*

39. On information and belief, Arastu has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, DDR3, LPDDR3, DDR4, and LPDDR4 systems that incorporate the Accused

Arastu Products. Arastu had the knowledge of the '069 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Arastu Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

40. On information and belief, Arastu has committed the foregoing infringing activities without a license.

41. On information and belief, Arastu's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

42. On information and belief, Arastu knew the '069 Patent existed, knew of an exemplary infringed claim of the '069 Patent, and knew of exemplary infringing Arastu products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT IV: INFRINGEMENT OF THE '603 PATENT

43. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

44. On information and belief, the Arastu Defendants have, individually, and jointly, infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States the Accused Arastu Products.

45. For example, on information and belief, Arastu has infringed at least claim 14 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of the Accused Arastu Products. The Accused Arastu Products include a multiplexer, such as the Command Buffer, the Bank

Management Unit, and/or the DFI Interface. Ex. 1 at 1. DDR3/4 Memory to which the Accused Arastu Products connect has multiple memory banks. The multiplexer in the Accused Arastu Products comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions, such as the inputs from AHB/AXI Slave buffers. *See* Ex. 1 at 1. The multiplexer also comprises a multiplexer output for sending each of the plurality of memory transactions to the memory, such as the DFI Status/Command and Data lines. *See* Ex. 1 at 1. Arastu receives a plurality of memory transactions at the multiplexer inputs. Each of the memory transactions is addressed to a corresponding memory bank. The Accused Arastu Products associate a priority with each received memory transaction. Ex. 1 at 2. ("Programmable Priority/QoS based system bus interface"). The Accused Arastu Products generate a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, such as following the submission of activate commands to the DDR4 memory. The bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output. *See* Ex. 1 at 2 ("Maximizes DRAM bus utilization by implementing Look-Ahead command processing and Bank Management"). Arastu sends each of the plurality of memory transactions to its corresponding memory bank via the DFI Interface Status/Command and Data lines based on the associated priorities and the bank readiness signals. *See* Ex. 1 at 1. *See also* Ex. 1 at 2 ("Programmable Priority/QoS based system bus interface" and "Maximizes DRAM bus utilization by implementing Look-Ahead command processing and Bank Management").

46. On information and belief, Arastu has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the

United States, DDR3, LPDDR3, DDR4, and LPDDR4 systems that incorporate the Accused Arastu Products. Arastu had the knowledge of the '603 Patent and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the Accused Arastu Products, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

47. On information and belief, Arastu has committed the foregoing infringing activities without a license.

48. On information and belief, Arastu's infringing activities commenced at least six years prior to the filing of this complaint, entitling CCO to past damages.

49. Arastu knew the '603 Patent existed, knew of its claims, and knew of Arastu's infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against the Arastu Defendants, and specifically, for the following relief:

A. Entry of judgment in favor of CCO against the Arastu Defendants on all counts;

B. Entry of judgment that the Arastu Defendants have infringed the Patents-in-Suit;

C. Entry of judgment that the Arastu Defendants' infringement of the Patents-in-Suit has been willful;

D. Award of compensatory damages adequate to compensate CCO for the Arastu Defendants' infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;

E. Declaration and finding that the Arastu Defendants' conduct in this case is

exceptional under 35 U.S.C. § 285;

F. Award of reasonable attorneys' fees and expenses against the Arastu Defendants pursuant to 35 U.S.C. § 285;

G. Award of CCO's costs;

H. Pre-judgment and post-judgment interest on CCO's award; and

I. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Dated: June 26, 2019

Respectfully submitted,

/s/ Dmitry Kheyfits

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